REMARKS

Claims 1-5 and 7-25 are currently active.

The Examiner has rejected Claims 1-5, 7-17 and 19 under 35 U.S.C. 112, second paragraph. The claims have been amended to obviate this rejection. Please note in Claim 15, it already states the "width of the carrier mechanism."

The Examiner has rejected Claims 1-5, 15, 16 and 18-21 as being unpatentable over Haddock in view of Nelson. Applicant respectfully traverses this rejection.

Referring to Haddock, there is disclosed a sliced comparison engine architecture and method for a LAN switch. The teachings of Haddock are directed to a scalable data path architecture and a data comparison engine utilized in filtering and forwarding data packets by a LAN switch operating in high speed LANs such as a gigabit Ethernet LAN. See column 1, lines 20-24. The switch 100 implements a central shared memory-based architecture that supports multiple high-speed ports or Macs 110. Each channel is capable of supporting one full-duplex gigabit Ethernet MAC, wherein a receive data path 111a receives data and a transmit data path 111b transmits data. The paths are further sliced into multiple sub paths over which data is routed by path controller 120 into the shared central memory or packet

memory 130, according to commands received from packet queue manager 160. See column 5, lines 44-66.

A forwarding data base 140 contains tables related to packets for flow identification, forcing and filtering, and stores the tables addresses and other well known fields obtained from packets transferred by path controller 120. A packet forwarding controller 150 maintains the tables in data base 140 and decides which packets or flows are identified, filtered, or forwarded, utilizing a comparison engine sliced according to an association with each of the number of sub path controllers. See column 6, lines 6-15.

Haddock teaches m-bit wide receiver data paths 111 through 114 couple Macs 110 to path controller 120. Path controller 120 is sliced into a number of sub paths controllers. Likewise, paths 111 through 114 are sliced into an equal number of n-bit wide receiver data sub paths, wherein n times the number of sub path controllers equals m. Each sub path belonging to a particular path is routed to a different sub path controller. The sub path controllers 120 are each coupled to packet memory 130 via a respective X-bit wide receive data bus 121. In one embodiment, the width of data bus 121 connecting the sub path controllers to packet memory 130 is double the sum of the width of the receive and transmit data paths coupling the Macs to path controller 120. See column 6, lines 17-50.

The sub path controllers each contain separate receive buffers coupled to each sub path to receive data therefrom. In the receive data direction each sub path controller accumulates at least X bits of data in the receive buffer from its associated receive data sub path until it can transfer the bits of data to packet memory 130, wherein X is a multiple of n. See column 6, lines 54-60.

The receive buffers operate as serial-to-parallel bit stream converters, and burst X bits of data in parallel to packet memory. The X bits contain n-bit slices of a data packet received from a MAC connected to the corresponding sub path. The data streams from each sub path are written to memory under the control of packet queue manager 160. Packet queue manager 160 generates the memory address locations at which the slices of data received from the Macs are stored in packet memory 130. A selector in respective sub path controllers 120 simultaneously selects receive buffers corresponding to the sub-paths of the same path and forwards the slices of data held therein to packet memory 130 over data bus 121. See column 7, lines 4-17.

M-bit wide transmit data paths 111 through 114 couple path controller 120 to Macs 110. As in the case of the receive data paths discussed above, the transmit data paths operate in a similar but opposite manner with respect to the receive data direction. The sub path controllers each read X-bit bursts from packet memory 130 over data bus 121, wherein

each burst represents multiple slices of a data packet. The sub path controllers send the data on the sub paths corresponding to a particular MAC. See column 7, lines 35-50.

Furthermore, there is no teaching or suggestion of "said providing mechanism transferring more than one packet at a time to the memory mechanism in the allocated time slot only when there is enough data from more than one packet from an input stage queue group to fill the width but not transferring any data from any packets from the input stage queue groups in the allocated time slot when there is not enough data to fill the width of the carrier mechanism," as found in Claim 1. The statement that the Examiner relies upon in Haddock simply states that each sub path controller accumulates at least x bits of data in the receive buffer from its associated receive data sub path until it can transfer the bits of data to packet memory 130, wherein x is a multiple of the number of bits in the receive data sub path. See column 6, lines 57-61. Just by the simple use of the language of "at least" x bits, indicates that more than x bits can be accumulated and sent to packet memory 130, which means that there are times when only x bits, that is, less than the total number of bits that can be transferred, are transferred, and thus the width of the path is not filled, at such times. Accordingly, for this reason, it is respectfully submitted that Haddock does not meet any of the limitations that the examiner states they do. Since the primary reference the Examiner cites does not support the Examiner's position regarding the above quoted limitations, then the reference of Nelson which also does not teach or suggest these limitations, but that is cited by

the Examiner for the proposition that it teaches to carry packets in the allocated time slot, in combination with Haddock fails to meet the limitations of applicant's claims. Accordingly, Claims 1-5, 15, 16 and 18-21 are patentable over Haddock in view of Nelson for this reason alone.

Referring to Nelson, there is disclosed a data communication system utilizing a scalable, non-blocking, high bandwidth central memory controller and method. Nelson teaches a central memory switch 10 comprises a dual port memory 12 which may comprise a plurality of 2-port static random access memory integrated circuits. The dual port memory 12 has an input port coupled to a TDM input bus 14 for coupling a plurality of assembly registers 16 corresponding to ports 1 through n respectively by means of an input holding register 18. The dual port memory 12 also has a outport coupled to a TDM output bus 20 through an output holding register 22 to provide output to a plurality of holding registers 24 corresponding to ports 1 through n respectively. A switch controller 26 operatively controls the functionality of the dual port memory 12. See column 3, line 52-column 4, line 5.

The centralized queuing structure of the central memory switch 10 accommodates all of the queue management functions for all of the input and output ports. The data is concatenated when a frame is received. Then, a request is raised to the switch controller 26 at the proper TDM cycle identifying that the data is available as well as its

intended destination queue. The switch controller 26 manipulates and manages a count of entries and supplies the prepared address to the dual port memory 12. See column 4, lines 5-17.

As is clear from the above description, Nelson also fails to teach or suggest the limitation of transferring more than one packet at a time to the memory mechanism only when there is enough data for more than one packet from an input stage queue to fill the width but not transferring any data from any packets from the input stage queue groups when there is not enough data to fill the width of the carrier mechanism. In fact, in regard to Nelson, it does not seem to be the slightest concern whatsoever of anything in regard to this limitation.

Moreover, since the Examiner is combining Haddock and Nelson, to arrive at applicant's claimed invention, there must be some teaching or suggestion in the references themselves to combine the teachings the Examiner is relying upon, and here, there is none.

It is respectfully submitted that the Examiner is using hindsight to arrive at applicant's claimed invention, but hindsight is not patent law. It is respectfully submitted the Examiner cannot use the limitations of Claim 1 as a road map to find the different limitations and disparate references, and having found the different teachings in the different references, concludes that applicant's claimed invention is arrived at.

Furthermore, teachings that the Examiner relies upon from the different references, cannot be taken out of the context in which they are found. Haddock teaches that a data path controller 120 is used to route the data into the packet memory 130. As shown in figure 2a, from each path controller 120, there is a respective data bus 121 that goes into a corresponding portion of the packet memory 130. In contrast, Nelson teaches a single TDM bus connects all the ports to the dual port memory 12. It is at the dual port memory 12 with the switch controller 26 that the functionality of the dual port memory 12 is controlled. This is in direct contrast to the data path controller 120 of Haddock which controls the data directly from the ports and not in the dual port memory 12 of Nelson as opposed to the packet memory 130 of Haddock. Accordingly, the architectures are distinct, and the bus that the Examiner relies on, taught by Nelson, is specifically useful in the architecture of the system taught by Nelson. These distinct contexts cannot be ignored.

In addition, it will be no simple matter to redesign the architecture shown in figure 2a of Haddock to somehow or other accommodate the TDM bus to provide the data to the respective corresponding portions of the packet memory 130. In fact, it goes specifically against the teachings of Haddock which call for the corresponding portion or sub path controller 120 to have its own corresponding data bus 121 that is directed into a corresponding packet memory portion 130. It would require significant research and development to figure out how to somehow or other replace the TDM bus for the individual corresponding data bus

121 so that the desired data from a sub path controller 120 finds its way into the corresponding portion of the packet memory. However, it is respectfully submitted this would make no sense and in fact destroy the whole purpose of trying to create an architecture of separate sub parts so they align and increase the efficiency of the architecture taught by Haddock. Accordingly, Claims 1-5, 15, 16 and 18-21 are patentable and over Haddock in view of Nelson.

The Examiner has rejected Claims 7-14, 17 and 22-25 as being unpatentable over Haddock in view of Nelson and Fukano. Applicant had discussed Fukano in the previous Office Action. Fukano does not add anything to the teachings of Haddock or Nelson to arrive at the above quoted limitations. Accordingly, these claims are patentable over Haddock in view of Nelson and Fukano.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-5 and 7-25, now in this application be allowed.

Respectfully submitted,

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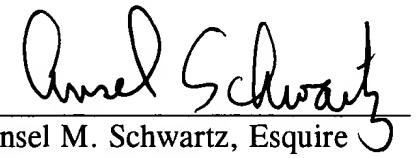
By 

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